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TITLE: Planar substrate with selected semiconductor crystal orientations formed by localized amorphization and recrystallization of stacked template layers

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Application Filing Date - APD (1):
**20031202**

Claims Text - CLTX (2):
1. A planar hybrid-orientation semiconductor-on-insulator (**SOI**) substrate structure comprising: at least two clearly defined **single crystal** semiconductor regions with different surface orientations, said at least two clearly defined **single crystal** semiconductor regions disposed on a common **buried** insulating layer, said common **buried** insulating layer disposed on a substrate.

Claims Text - CLTX (3):
2. The planar hybrid-orientation **SOI** substrate structure of claim 1 further comprising at least one isolation region separating said at least two clearly defined **single crystal** semiconductor regions from each other.

Claims Text - CLTX (4):
3. The planar hybrid-orientation **SOI** substrate structure of claim 2 wherein said at least one isolation region is a **trench** isolation region.

Claims Text - CLTX (5):
4. The planar hybrid-orientation **SOI** substrate structure of claim 2 wherein said at least one isolation region extends down to at least an upper surface of the common **buried** insulating layer.

Claims Text - CLTX (6):
5. The planar hybrid-orientation **SOI** substrate structure of claim 2 wherein said at least one isolation region does not extend down to said common **buried** insulating layer.

Claims Text - CLTX (7):
6. The planar hybrid-orientation **SOI** substrate structure of claim 1 wherein said at least two clearly defined **single crystal** semiconductor regions comprise

the same or different semiconductor materials.

Claims Text - CLTX (8):
7. The planar hybrid-orientation **SOI** substrate structure of claim 6 wherein said semiconductor materials are selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.

Claims Text - CLTX (9):
8. The planar hybrid-orientation **SOI** substrate structure of claim 1 wherein said at least two clearly defined **single crystal** semiconductor regions with different surface orientations both comprise a Si-containing semiconductor material.

Claims Text - CLTX (10):
9. The planar hybrid-orientation **SOI** substrate structure of claim 1 wherein said at least two clearly defined **single crystal** semiconductor regions are each comprised of strained, unstrained or a combination of strained and unstrained semiconductor materials.

Claims Text - CLTX (11):
10. The planar hybrid-orientation **SOI** substrate structure of claim 1 wherein said different surface orientations are selected from the group consisting of (110), (111) and (100).

Claims Text - CLTX (12):
11. The planar hybrid-orientation **SOI** substrate structure of claim 8 wherein said different surface orientations are selected from the group consisting of (110), (111) and (100).

Claims Text - CLTX (13):
12. The planar hybrid-orientation **SOI** substrate structure of claim 11 wherein said first Si-containing semiconductor region has a (100) crystal orientation and said second Si-containing semiconductor region has a (110) crystal orientation.

Claims Text - CLTX (14):
13. The planar hybrid-orientation **SOI** substrate structure of claim 12 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on said (100) crystal orientation and said at least pFET device is located on said (110) crystal orientation.

Claims Text - CLTX (15):
14. The planar hybrid-orientation **SOI** substrate structure of claim 1 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

Claims Text - CLTX (16):
15. The planar hybrid-orientation **SOI** substrate structure of claim 1 wherein said **buried** insulating layer is a dielectric material selected from the group consisting of SiO.sub.2, crystalline SiO.sub.2, SiO.sub.2 containing nitrogen, silicon **nitride,** metal **oxides,** metal **nitrides,** and highly thermally conductive materials.

Claims Text - CLTX (17):
16. The planar hybrid-orientation **SOI** substrate structure of claim 15 wherein said dielectric material is SiO.sub.2 or crystalline SiO.sub.2.

Claims Text - CLTX (18):
17. The planar hybrid-orientation **SOI** substrate structure of claim 1 wherein said substrate is a semiconductor material selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.

Claims Text - CLTX (19):
18. The planar hybrid-orientation **SOI** substrate structure of claim 1 wherein said substrate has an epitiaxial relationship to at least one of said **single crystal** semiconductor regions.

Claims Text - CLTX (20):
19. The planar hybrid-orientation **SOI** substrate structure of claim 1 wherein said at least two clearly defined **single crystal** semiconductor regions comprise three **single crystal** semiconductor regions of different **crystal** orientation that are separated by isolation regions.

Claims Text - CLTX (21):
20. The planar-hybrid-orientation **SOI** substrate structure of claim 19 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal

orientation that is optimal for said device.

Claims Text - CLTX (22):
21. The planar-hybrid-orientation **SOI** substrate structure of claim 1 wherein at least one of said at least two clearly defined **single crystal** regions comprises an upper semiconductor disposed on a lower, residual semiconductor, said upper and lower semiconductors having different surface orientations, said residual semiconductor in direct contact with said common **buried** insulating layer.

Claims Text - CLTX (23):
22. The planar-hybrid-orientation **SOI** substrate structure of claim 21 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

Claims Text - CLTX (24):
23. The planar hybrid-orientation **SOI** substrate structure of claim 21 further comprising at least one isolation region separating said at least two clearly defined **single crystal** semiconductor regions from each other, wherein said at least one isolation region extends down at least to said common **buried** insulating layer.

Claims Text - CLTX (25):
24. The planar hybrid-orientation **SOI** substrate structure of claim 21 further comprising at least one isolation region separating said at least two clearly defined **single crystal** semiconductor regions from each other, wherein said at least one isolation region does not extend down to said common **buried** insulating layer.

Claims Text - CLTX (26):
25. The planar hybrid-orientation **SOI** substrate structure of claim 1 wherein said substrate is an insulator.

Claims Text - CLTX (27):
26. The planar hybrid-orientation **SOI** substrate structure of claim 8 wherein at least one of said at least two clearly defined **single crystal** Si-containing semiconductor regions comprises an upper Si-containing semiconductor disposed on a lower, residual Si-containing semiconductor, said upper and lower semiconductors having different surface orientations, said residual semiconductor in direct contact with said common **buried oxide** layer.

Claims Text - CLTX (28):
27. The planar hybrid-orientation **SOI** substrate structure of claim 26 wherein said different surface orientations are selected from the group consisting of (110), (111) and (100).

Claims Text - CLTX (29):
28. The planar hybrid-orientation **SOI** substrate structure of claim 27 wherein first Si-containing semiconductor region has a (100) crystal orientation and said second Si-containing semiconductor region has a (110) crystal orientation.

Claims Text - CLTX (30):
29. The planar hybrid-orientation **SOI** substrate structure of claim 28 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on said (100) crystal orientation and said at least pFET device is located on said (110) crystal orientation.

Claims Text - CLTX (31):
30. The planar hybrid-orientation **SOI** substrate structure of claim 26 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

Claims Text - CLTX (32):
31. The planar hybrid-orientation **SOI** substrate structure of claim 26 further comprising at least one isolation region separating said at least two clearly defined **single crystal** Si-containing semiconductor regions from each other.

Claims Text - CLTX (33):
32. The planar hybrid-orientation **SOI** substrate structure of claim 31 wherein said at least one isolation region is a **trench** isolation region.

Claims Text - CLTX (34):
33. The planar hybrid-orientation **SOI** substrate structure of claim 31 wherein said at least one isolation region extends down to at least an upper surface of the common **buried** insulating layer.

Claims Text - CLTX (35):

Claims Text - CLTX (28):
27. The planar hybrid-orientation **SOI** substrate structure of claim 26 wherein said different surface orientations are selected from the group consisting of (110), (111) and (100).

Claims Text - CLTX (29):
28. The planar hybrid-orientation **SOI** substrate structure of claim 27 wherein first Si-containing semiconductor region has a (100) crystal orientation and said second Si-containing semiconductor region has a (110) crystal orientation.

Claims Text - CLTX (30):
29. The planar hybrid-orientation **SOI** substrate structure of claim 28 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on said (100) crystal orientation and said at least pFET device is located on said (110) crystal orientation.

Claims Text - CLTX (31):
30. The planar hybrid-orientation **SOI** substrate structure of claim 26 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

Claims Text - CLTX (32):
31. The planar hybrid-orientation **SOI** substrate structure of claim 26 further comprising at least one isolation region separating said at least two clearly defined **single crystal** Si-containing semiconductor regions from each other.

Claims Text - CLTX (33):
32. The planar hybrid-orientation **SOI** substrate structure of claim 31 wherein said at least one isolation region is a **trench** isolation region.

Claims Text - CLTX (34):
33. The planar hybrid-orientation **SOI** substrate structure of claim 31 wherein said at least one isolation region extends down to at least an upper surface of the common **buried** insulating layer.

Claims Text - CLTX (35):

34. The planar hybrid-orientation **SOI** substrate structure of claim 31 wherein said at least one isolation region does not extend to said common **buried oxide** layer.

Claims Text - CLTX (36):
35. A method of forming a planar hybrid-orientation substrate comprising the steps of forming a bilayer template layer stack comprising a first, lower **single crystal** semiconductor layer having a first orientation and a second, upper **single crystal** semiconductor layer having a second orientation different from the first; amorphizing one of the semiconductor layers of the bilayer template stack in selected areas to form localized amorphized regions; and recrystallizing the localized amorphized regions using a non-amorphized semiconductor layer of the stack as a template, thereby changing the orientation in the localized amorphized regions from an original orientation to a desired orientation.

Claims Text - CLTX (37):
36. The method of claim 35 wherein said first, lower **single crystal** semiconductor layer is disposed on the insulating layer of an **SOI** substrate.

Claims Text - CLTX (38):
37. The method of claim 35 wherein said first, lower **single crystal** semiconductor layer comprises a **single crystal** semiconductor substrate.

Claims Text - CLTX (39):
38. The method of claim 35 wherein said second, upper **single crystal** semiconductor layer is formed atop the first, lower **single crystal** semiconductor by bonding.

Claims Text - CLTX (40):
39. The method of claim 35 wherein said localized amorphized region is formed predominately within the second, upper **single crystal** semiconductor layer.

Claims Text - CLTX (41):
40. The method of claim 35 wherein said localized amorphized region is formed predominately within the first, lower **single crystal** semiconductor layer.

Claims Text - CLTX (42):
41. The method of claim 36 wherein said localized amorphized region is formed predominately within the first, lower **single crystal** semiconductor

layer, and further including the step of removing said top layer after recrystallization, by a process such as chemical mechanical polishing.

Claims Text - CLTX (43):
42. The method of claim 35 further comprising forming at least one **trench** isolation region to separate said areas selected for amorphization from those not selected for amorphization, said at least one **trench** isolation being formed prior to amorphizing, between amorphizing and recrystallizing, or partially after amorphizing and partially after recrystallizing.

Claims Text - CLTX (44):
43. The method of claim 35 wherein said first, lower **single crystal** semiconductor and layer said second, upper **single crystal** semiconductor layer are composed of the same or different semiconductor material selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.

Claims Text - CLTX (45):
44. The method of claim 35 wherein said first, lower **single crystal** semiconductor layer and said second, upper **single crystal** semiconductor layer are both composed of a Si-containing semiconductor material.

Claims Text - CLTX (46):
45. The method of claim 35 wherein said first, lower **single crystal** semiconductor layer and said second, upper **single crystal** semiconductor layer are composed of strained, unstrained or a combination of strained and unstrained semiconductor materials.

Claims Text - CLTX (47):
46. The method of claim 35 wherein said first, lower **single crystal** semiconductor layer and said second, upper **single crystal** semiconductor layer have different surface orientations selected from (110), (111) and (100).

Claims Text - CLTX (49):
48. The method of claim 37 further comprising forming a **buried** insulating layer after said recrystallizing step.

Claims Text - CLTX (50):
49. The method of claim 48 wherein said **buried** insulating layer is formed by a separation-by-ion implantation of oxygen (SIMOX) process.